ABSTRACT OF THE DISCLOSURE

A hardware unit (2) for operating memory components comprises a memory controller, a bus and a plurality of interface pins 3-6. The bus is connected to the memory controller and to the interface pins. In order to enable a flexible employment of the hardware unit, the memory controller determines the number of memory components (21,31,41,42,51,52,61,62) connected to the interface pins. In case at least one memory component is determined, the memory controller divides the capacity of the bus into as many portions as there are connected memory components, allocates each portion to another group of interface pins to which a separate memory component is connected, and exchanges signals via the bus and the interface pins separately with each connected memory component. The invention relates equally to an electronic device 1 comprising such a hardware unit and to a corresponding method.

For publication: Figure 1